wherein the first processor is configured to operate at a first frequency, the second processor is configured to operate at a second frequency, and the first frequency is greater than the second frequency, and wherein the first bus and the second bus are dissimilar.

18. (New) The electronic product of Claim 17, wherein the first processor and the second processor are both disposed together on a single integrated circuit.

19. (New) The electronic product of Claim 18, wherein the first processor is a digital signal processor, and the second processor is a microcontroller.

20. (New) The electronic product of Claim 19, wherein a first portion of the first memory is dedicated to the first processor, a second portion of the first memory is dedicated to the second processor, and a third portion of the first memory is shared by the first and the second processors.

21. (New) The electronic product of Claim 20, wherein the first bus has a first width, the second bus has a second width, and the third bus has a third width; the first width is greater than the second width, and the second width is greater than the third width.

22. (New) The electronic product of Claim 21, wherein the DMA controller and the second bus are both disposed on the single integrated circuit.

23. (New) The electronic product of Claim 22, wherein the first bus has a width of 128 bits, the second bus has a width of 32 bits, and the third bus has a width of 16 bits.

24. (New) The electronic product of Claim 22, further comprising a Read Only Memory (ROM) disposed on the single integrated circuit and coupled to the second bus.

25. (New) A mobile radiotelephony controller, comprising:

a digital signal processor coupled to an instruction cache and to a data cache;

a first bus coupled to the instruction cache and to the data cache;

a first memory coupled to the first bus;

a microcontroller coupled to a second bus;

a first bus bridge coupled to the first bus and to the second bus, the first bus bridge providing a path for transferring data between the first memory and the microcontroller;

a second memory coupled to the first bus;

a second bus bridge coupled to the second bus and a third bus, the third bus providing a data pathway within the digital signal processor, the second bus bridge providing a path for transferring data between the second memory and the third bus of the digital signal processor; and

a direct memory access (DMA) controller coupled to the second bus, the DMA controller configured to manage a transfer of data between the second memory and the second bus bridge;

wherein the digital signal processor is configured to operate at a first frequency, the microcontroller is configured to operate at a second frequency, and the first frequency is greater than the second frequency, wherein the first bus and the second bus are dissimilar, and wherein a first portion of the first memory is dedicated to the digital signal processor, a second portion of the first memory is dedicated to the microcontroller, and a third portion of the first memory is shared by the digital signal processor and the microcontroller.

26. (New) The mobile radiotelephony controller of Claim 25, further comprising a ROM coupled to the second bus.

27. (New) The mobile radiotelephony controller of Claim 26, wherein the first bus has a first width, the second bus has a second width, and the third bus has a third width; the first width is greater than the second width, and the second width is greater than the third width.

28. (New) The mobile radiotelephony controller of Claim 27, wherein the digital signal processor, the microcontroller, the DMA controller, the ROM, the first memory, and the second memory are all disposed on the same single integrated circuit.